# Precision Analog Microcontroller with RF Transceiver, ARM Cortex™-M3

Preliminary Technical Data

# ADuCRF101

## FEATURES

**Analog I/O**
**6-Channel 14-bit or 12-bit ADC**
- Single ended and differential inputs
- Programmable data rate up to 842 kSPS
- On-Chip Voltage Reference and Temperature Sensor

**Power**
- Supply Range: 2.2 V to 3.6 V
- Power Consumption
  - 680 nA, in power down mode, non-retained state
  - 1.6 µA, in power down mode, processor memory and transceiver memory retained
  - 190 µA / MHz, Cortex in Active mode
  - 12.8 mA transceiver in receive mode, Cortex in power down mode
  - 9 mA to 32 mA transceiver in transmit mode, Cortex in power down mode

**RF Transceiver**
- Frequency bands
  - 862 MHz to 928 MHz
  - 431 MHz to 464 MHz
- Multiple Configurations supported
- Receiver sensitivity (BER)
  - -107.5 dBm at 38.4 kbps, 2FSK
- Single ended and differential PA
- Low External BOM

**Microcontroller**
- ARM Cortex™-M3 32-bit processor
- Serial Wire download and debug
- External Watch crystal for wakeup timer
- 16 MHz internal Oscillator with 8-way Programmable Divider

**Memory**
**128 k Bytes /64 k Bytes Flash/EE Memory, 16 k Bytes /8 k Bytes SRAM**
- 20000 cycle Flash/EE endurance
- 10 year Flash/EE retention
- In-circuit download via Serial Wire and UART

**On-Chip Peripherals**
- UART, I²C and SPI Serial I/O
- 28-Pin GPIO Port
- 2 General Purpose Timers
- Wake-up Timer
- Watchdog Timer
- 8-Channel PWM

**Packages and Temperature Range**
- 64 lead LFCSP (9mm x 9mm) package –40°C to 85°C

**Tools**
- Low-Cost Development System
- Third-Party Compiler and emulator tool Support

## APPLICATIONS

**Battery powered wireless sensor**
**Medical telemetry systems**
**Industrial and home automation**
**Asset tracking**
**Security systems (access systems)**
**Health and fitness applications**

## FUNCTIONAL BLOCK DIAGRAM

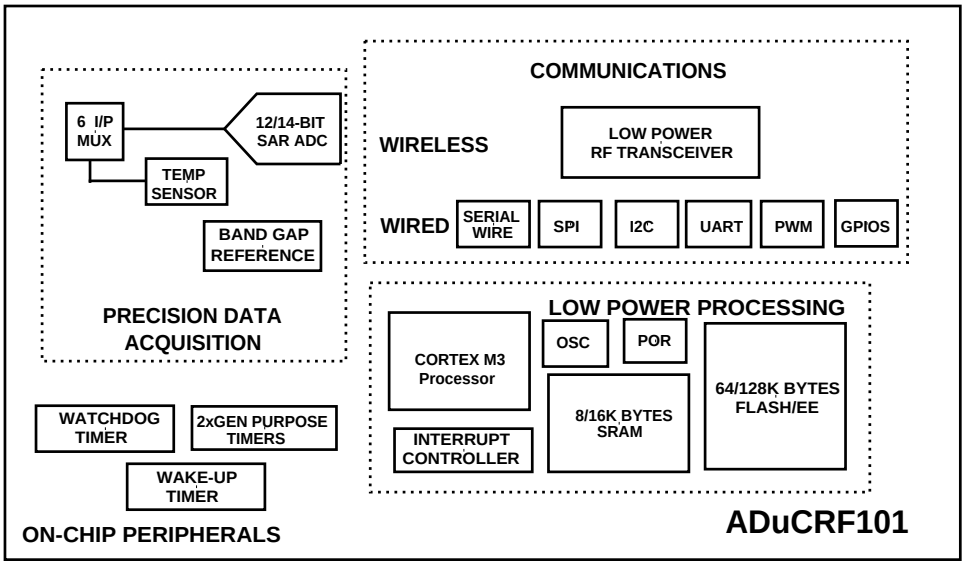


*Figure 1. ADuCF101 Block Diagram*

**Rev. PrG**


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# TABLE OF CONTENTS

# GENERAL DESCRIPTION

The ADuCRF101 is a fully integrated data acquisition solution designed for low power wireless applications. It features a 12-bit or 14-bit ADC, a low power Cortex™-M3 processor from ARM®, a 431 MHz to 464 MHz and 862 MHz to 928 MHz RF transceiver, and Flash/EE memory packaged in a 9 mm × 9 mm LFCSP.

The acquisition section consists of a 12-bit / 14-bit ADC SAR ADC. The six inputs can be configured as single ended or differential modes. When configured in single ended mode, they can be used for ratiometric measurements on sensors, powered when required from the internal LDO. An internal battery monitor channel and an on-chip temperature sensor are also available.

This wireless data acquisition system is designed to operate in battery-powered applications where low power is critical. The device can be configured in normal operating mode or different low power modes under direct program control. In flexi mode any peripheral can operate and wake-up the device. In hibernate mode the internal wake-up timer remains active. In shutdown mode only an external interrupt can wake-up the device.

The ADuCRF101 integrates a low power Cortex-M3 processor from ARM. It is a 32-bit RISC machine, offering up to 1.25 DMIPS peak performance. The Cortex-M3 processor also has a flexible 14-channel DMA controller supporting communication peripherals SPI, UART and $I^2C$. 64 kB / 128 kB of nonvolatile Flash/EE memory and 8 kB / 16 kB of SRAM are also provided on-chip.

A 16 MHz on-chip oscillator generates the system clock. This clock can be internally divided for the processor to operate at lower frequency for power saving reasons. A low power internal 32 kHz oscillator is available and can used to clock the timers. There are two general-purpose timers, a wake-up timer and a system watchdog timer.

A range of communication peripherals can be configured as required in a specific application. These peripherals include UART, $I^2C$, SPI, GPIO ports, PWM and RF transceiver.

The RF transceiver communicates in the 431 MHz to 464 MHz and 862 MHz to 928 MHz frequency bands using multiple configurations.

On-chip factory firmware supports in-circuit serial download via the UART while nonintrusive emulation and program download is also supported via the serial wire interface. These features are incorporated into a low cost development system supporting this precision analog microcontroller family.

The parts operate from 2.2 V to 3.6 V and are specified over an industrial temperature range of −40°C to +85°C.

Three versions of the ADuCRF101 are available:

- 14-bit ADC, 128 k Byte Flash and 16 k Byte SRAM
- 12-bit ADC, 128 k Byte Flash and 16 k Byte SRAM
- 12-bit ADC, 64 k Byte Flash and 8 k Byte SRAM

# SPECIFICATIONS

## ELECTRICAL SPECIFICATIONS

AVDD = IOVDD = VDDBAT1 = VDDBAT2 = 2.2 V to 3.6 V, $V_{REF}$ = 1.25 V internal reference, $f_{CORE}$ = 16 MHz, $T_A$ = −40°C to +85°C unless otherwise noted. Default ADC sampling frequency: eight acquisition clocks and ADC clock frequency of 4 MHz.

**Table 1. 12 Bit ADC channel specification**

| Parameter | Test Conditions / Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC ACCURACY | Single ended input mode. Applies to all ADC input channels. | | | | |
| Resolution | | | 12 | | Bits |
| Integral Nonlinearity | $V_{REF}$ = 1.25 V from internal reference | | ±1 | | LSB |
| | $V_{REF}$ = 1.8 V from LDO | | ±2 | | LSB |
| Differential Nonlinearity | Guaranteed no missing code | | ±1 | | LSB |
| DC Code Distribution | ADC input is a DC voltage | | 2 | | LSB |
| CALIBRATED ENDPOINT ERRORS | Measured using the factory-set default values ADCOF and ADCGN. | | | | |
| Offset Error | | | ±0.6 | | LSB |
| Offset Error Match | | | ±0.25 | | LSB |
| Gain Error | | | ±1.25 | | LSB |
| Gain Error Match | | | ±0.25 | | LSB |
| DYNAMIC PERFORMANCE | $f_{IN}$ = 10 kHz sine wave. | | | | |
| Signal-to-Noise Ratio (SNR) | | | 68 | | dB |
| Total Harmonic Distortion | | | TBD | | |
| Peak Harmonic or Spurious Noise (PHSN) | | | TBD | | |
| Channel-to-Channel Crosstalk | Measured on adjacent channels | | TBD | | |

**Table 2. 14 Bit ADC channel specification**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ADC SPECIFICATIONS | | | | | |
| DC ACCURACY | Single ended input mode. Applies to all ADC input channels. | | | | |
| Resolution | | | 14 | | Bits |
| Integral Nonlinearity | $V_{REF}$ = 1.25 V from internal reference | | ±4 | | LSB |
| | $V_{REF}$ = 1.8 V from LDO | | ±8 | | LSB |
| Differential Nonlinearity | Guaranteed no missing code | | ±1 | | LSB |
| DC Code Distribution | ADC input is a DC voltage | | 8 | | LSB |
| CALIBRATED ENDPOINT ERRORS | Measured using the factory-set default values ADCOF and ADCGN. | | | | |
| Offset Error | | | ±2.5 | | LSB |
| Offset Error Match | | | ±1 | | LSB |
| Gain Error | | | ±5 | | LSB |
| Gain Error Match | | | ±1 | | LSB |
| DYNAMIC PERFORMANCE | $f_{IN}$ = 10 kHz sine wave. | | | | |
| Signal-to-Noise Ratio (SNR) | | | 80 | | dB |
| Total Harmonic Distortion | | | TBD | | |
| Peak Harmonic or Spurious Noise (PHSN) | | | TBD | | |
| Channel-to-Channel Crosstalk | Measured on adjacent channels | | TBD | | |

**Table 3. ADuCRF101 Specification**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ADC SPECIFICATIONS | | | | | |
| ANALOG INPUT | | | | | |
| Input Voltage Ranges[1] | | | | | |
| Single ended input | | 0 | | $V_{REF}$ | V |
| Differential input | | 0 | | $V_{CM} \pm V_{REF}/2$ | V |
| Leakage Current | | | 100 | | nA |
| Input Capacitance | During ADC Acquisition | | 20 | | pF |
| ADC Power-up Time | Excludes reference power up time | | 5 | | µs |
| ON-CHIP VOLTAGE REFERENCE | | | | | |
| Output Voltage | | | 1.25 | | V |
| Accuracy | Measured at $T_A$ = 25°C | | ±5 | | mV |
| Reference Temperature Co | | | ±40 | | ppm/°C |
| Power Supply Rejection Ratio | | | 60 | | dB |
| Output Impedance | | | 2 | | Ω |
| Internal $V_{REF}$ Power-On Time | 0.47µF external capacitor | | 5 | | ms |
| TEMPERATURE SENSOR[1] | Indicates die temperature | | | | |
| Voltage Output at 25°C | | | TBD | | mV |
| Voltage TC | | | TBD | | mV/°C |
| Accuracy | MCU in low power mode | | TBD | | °C |
| Thermal impedance | | | TBD | | |
| CURRENT CONSUMPTION | RF transceiver in sleep mode, memory not retained | | | | |
| Cortex in SHUTDOWN mode | Wake up timer running from external 32 kHz crystal, 8 kB of SRAM retained (8 kB non-retained) | | 680 | | nA |
| Cortex in HIBERNATE mode | | | | | |
| RF transceiver in sleep mode, memory retained | | | 1.6 | | µA |
| RF transceiver in sleep mode, memory not retained | | | 1.38 | | µA |
| RF transceiver in receive mode | | | 12.8 | | mA |
| RF transceiver in transmit mode | | | 9 to 32 | | mA |
| Cortex in ACTIVE mode | RF transceiver idle (PHY_ON or PHY_OFF) | | | | |
| Static current | | | 1.8 | | mA |
| Dynamic current | | | 190 | | µA/MHz |
| STARTUP TIME[1] | From applying power/asserting active external interrupt to user code execution | | | | |
| From Power On and SHUTDOWN mode | FCLK is the Cortex-M3 clock or divided version of the 16 MHz oscillator. | | 50 | | ms |
| From FLEXI mode | From wake up event to user code execution | | 3 to 5 | | FCLK |
| From HIBERNATE mode | Includes 310 µs for 26 MHz crystal start up (7 pF load capacitor at $T_A$ = 25 °C) | | 12.5 | | µs |
| RF link waking up from sleep mode | | | 562.8 | | µs |
| POWER SUPPLY REQUIREMENTS | | | | | |
| Power Supply Voltage Range[1] | | 2.2 | | 3.6 | V |
| POWER SUPPLY MONITOR | | | | | |
| Trip Point voltage | | | 2 | | V |
| POWER-ON-RESET | | | 1.67 | | V |
| Watchdog Timer[1] | | | | | |
| Timeout Period | Programmable | 0 | | 512 | S |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Flash/EE MEMORY [1] | | | | | |
| Endurance[2] | | 20,000 | | | Cycles |
| Data Retention[3] | $T_J$ = 85°C | 10 | | | Years |
| Digital Inputs | All digital inputs, excluding LFXTAL1 and XOSC26P | | | | |
| Input Current (leakage current) | $V_{INH}$ = IOVDD or $V_{INH}$ = 2.2V, pull up disabled. $V_{INL}$ = 0V, pull up disabled. | | 10 | | nA |
| Input Capacitance | | | 10 | | pF |
| Logic Inputs | All Logic inputs, including LFXTAL1, excluding XOSC26P | | | | |
| VINL, Input Low Voltage | | | | 0.2 x IOVDD | V |
| VINH, Input High Voltage | | 0.7 x IOVDD | | | V |
| Logic Outputs | | | | | |
| VOH, Output High Voltage | $I_{source}$ = 1 mA | IOVDD – 0.4 | | | V |
| VOL, Output Low Voltage | $I_{sink}$ = 1 mA | | | 0.36 | V |
| 32.768 kHz CRYSTAL | 32.768 kHz crystal, for use with timers and/or RF transceiver wake up controller. | | | | |
| Input Current (leakage current) | $V_{INH}$ = IOVDD or $V_{INH}$ = 2.2 V $V_{INL}$ = 0 V. | | 50 | | nA |
| LFXTAL1 Input Capacitance | | | 2 | | pF |
| LFXTAL2 Output Capacitance | | | 2 | | pF |
| 26 MHz CRYSTAL | | | | | |
| XOSC26P Input Capacitance | | | 10 | | pF |
| XOSC26N Output Capacitance | | | 10 | | pF |
| INTERNAL HF OSCILLATOR | Processor clock by default | | 16 | | MHz |
| Tolerance | | | ±3 | | % |
| INTERNAL LF OSCILLATOR | | | 32.768 | | kHz |
| Tolerance | | | ±20 | | % |
| MCU CLOCK DIVIDER[1] | 8 programmable core clock dividers. | 1 | | 128 | |
| EXTERNAL CLOCK INPUT1 | External MCU clock range allowed | | | | |
| Range | | 32.768 | | 16000 | kHz |
| **RF LINK SPECIFICATIONS** | | | | | |
| FREQUENCY RANGE | | 862 | | 928 | MHz |
| | | 431 | | 464 | MHz |
| PHASE-LOCKED LOOP | | | | | |
| Channel Frequency Resolution | | | 396.7 | | Hz |
| Phase Noise (In-Band) | 10 kHz offset, PA output power = 10 dBm | | -88 | | dBc/Hz |
| DATA RATE | | | | | |
| 2FSK | | 1 | | 300 | kbps |
| OOK | Manchester Encoding enabled (Manchester chip rate = 2 x datarate) | 2.4 | | 19.2 | kbps |
| Data rate resolution | | | 100 | | bps |
| DIFFERENTIAL PA | | | | | |
| Transmit Power[4] | Programmable. | | -17 to 10 | | dBm |
| Transmit Power variation V's Temperature | From -40 °C to +85 °C, RF Frequency = 868 MHz | | ±1 | | dB |
| Transmit Power Flatness | From 902 MHz to 928 MHz and 863 MHz to 870 MHZ | | ±1 | | dB |
| SINGLE ENDED PA | | | | | |
| Transmit Power[4] | Programmable. | | -21 to 13 | | dBm |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Transmit Power variation V's Temperature | From -40°C to +85°C, RF Frequency = 868 MHz | | ±0.5 | | dB |
| Transmit Power Flatness | From 431 MHz to 464 MHz and 862 MHz to 928 MHZ | | ±1 | | dB |
| HARMONICS | 868 MHz, unfiltered conductive, PA output power = 10 dBm | | | | |
| Differential PA | | | | | |
| Second Harmonic | | | TBD | | dBc |
| Third Harmonic | | | TBD | | dBc |
| All Other Harmonics | | | TBD | | dBc |
| OPTIMUM PA LOAD IMPEDANCE | | | | | |
| Single-Ended PA, in Transmit Mode | | | | | |
| $f_{RF}$ = 915 MHz | | | 31.2+j10.4 | | Ω |
| $f_{RF}$ = 868 MHz | | | 23.5+j9.7 | | Ω |
| $f_{RF}$ = 433 MHz | | | 35.4+j3.4 | | Ω |
| Differential PA, in Transmit Mode | Load impedance between RFIO_1P and RFIO_1N to ensure maximum output power | | | | |
| $f_{RF}$ = 915 MHz | | | 38.7+j20.6 | | Ω |
| $f_{RF}$ = 868 MHz | | | 42.2+j20.1 | | Ω |
| $f_{RF}$ = 433 MHz | | | 55.6+j54.9 | | Ω |
| MODULATION | | | | | |
| Deviation Frequency Resolution | | | 100 | | Hz |
| 2FSK/GFSK INPUT SENSITIVITY, BIT ERROR RATE (BER) | At BER = $10^{-3}$ | | | | |
| 1.0 kbps | Frequency deviation = 10 kHz, IF filter bandwidth = 100 kHz | | -116 | | dBm |
| 38.4 kbps | Frequency deviation = 19.2 kHz, IF filter bandwidth = 100 kHz | | -107.5 | | dBm |
| 300 kbps | Frequency deviation = 75 kHz, IF filter bandwidth = 300 kHz | | -100.5 | | dBm |
| 2FSK/GFSK INPUT SENSITIVITY, PACKET ERROR RATE (PER) | At PER = 1%, packet length =20 bytes, packet mode | | | | |
| 1.0 kbps | Frequency deviation = 10 kHz, IF filter bandwidth = 100 kHz | | -115.5 | | dBm |
| 38.4 kbps | Frequency deviation = 19.2 kHz, IF filter bandwidth = 100 kHz | | -106 | | dBm |
| 300 kbps | Frequency deviation = 75 kHz, IF filter bandwidth = 300 kHz | | -98 | | dBm |
| ADJACENT CHANNEL REJECTION | | | | | |
| CW Interferer | Wanted signal 3 dB above the input sensitivity level (BER = $10^{-3}$), CW interferer power level increased until BER = $10^{-3}$, image calibrated | | | | |
| 200 kHz Channel Spacing | IF BW = 100 kHz, wanted signal: $F_{DEV}$ = 12.5 kHz, DR = 50 kbps | | 38 | | dB |
| 300 kHz Channel Spacing | IF BW = 100 kHz, wanted signal: $F_{DEV}$ = 25 kHz, DR = 100 kbps | | 39 | | dB |
| 600 kHz Channel Spacing | IF BW = 300 kHz, wanted signal: $F_{DEV}$ = 75 kHz, DR = 300 kbps | | 41 | | dB |
| Modulated Interferer | Wanted signal 3 dB above the input sensitivity level (BER = $10^{-3}$), modulated interferer with the same modulation as the wanted signal; interferer power level increased until BER = $10^{-3}$, image calibrated | | | | |
| 200 kHz Channel Spacing | IF BW = 100 kHz, wanted signal: $F_{DEV}$ = | | 38 | | dB |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| | 12.5 kHz, DR = 50 kbps | | | | |
| 300 kHz Channel Spacing | IF BW = 100 kHz, wanted signal: $F_{DEV}$ = 25 kHz, DR = 100 kbps | | 36 | | dB |
| 600 kHz Channel Spacing | IF BW = 300 kHz, wanted signal: $F_{DEV}$ = 75 kHz, DR = 300 kbps | | 35 | | dB |
| CO-CHANNEL REJECTION | Desired signal 10 dB above the input sensitivity level (BER = $10^{-3}$), data rate = 38.4 kbps, frequency deviation = 20 kHz. | | -4 | | dB |
| BLOCKING, ETSI EN 300 220 | Measurement procedure as per ETSI EN 300 220-1 V2.3.1; desired signal 3 dB above the ETSI EN 300 220 reference sensitivity level of −99 dBm, IF bandwidth =100 kHz, data rate = 38.4 kbps, unmodulated interferer. | | | | |
| ±2 MHz | | | -28 | | dBm |
| ±10 MHz | | | -20.5 | | dBm |
| WIDEBAND INTERFERENCE REJECTION | Swept from 10 MHz to 100 MHz either side of the RF frequency | | 75 | | dB |
| IMAGE CHANNEL ATTENUATION | Measured as image attenuation at the IF filter output, carrier wave interferer at 400 kHz below the channel frequency, 100 kHz IF filter bandwidth | | | | |
| 868 MHz | Uncalibrated[5]/calibrated | | 36/45 | | dB |
| RSSI | | | | | |
| Range at Input | | | −97 to −26 | | dBm |
| Linearity | | | ±2 | | dB |
| Absolute Accuracy | | | ±3 | | dB |
| LNA INPUT IMPEDANCE | | | | | |
| Receive Mode | | | | | |
| $f_{RF}$ = 915 MHz | | | 68.9-j36.1 | | Ω |
| $f_{RF}$ = 868 MHz | | | 71.6-j36.4 | | Ω |
| $f_{RF}$ = 433 MHz | | | 99.2-j31.3 | | Ω |
| Transmit Mode | | | | | |
| $f_{RF}$ = 915 MHz | | | 8.6+j21.1 | | Ω |
| $f_{RF}$ = 868 MHz | | | 8.6+j20.4 | | Ω |
| $f_{RF}$ = 433 MHz | | | 8.2+j11.4 | | Ω |
| RX SPURIOUS EMISSIONS | | | | | |
| Maximum <1 GHz | At antenna input, unfiltered conductive | | TBD | | dBm |
| Maximum >1 GHz | At antenna input, unfiltered conductive | | TBD | | dBm |

[1] These numbers are not production tested, but are guaranteed by design and/or characterization data at production release.
[2] Endurance is qualified to 20,000 cycles as per JEDEC Std. 22 Method A117 and measured at −40°C, +25°C, and +85°C. Typical endurance at 25°C is 170,000 cycles.
[3] Retention lifetime equivalent at a junction temperature ($T_J$) of 85°C as per JEDEC Std. 22 Method A117. Retention lifetime derates with junction temperature.
[4] Measured as the maximum unmodulated power.
[5] Measured with IMAGE_REJECT_CAL_AMPLITUDE = 0x7 and IMAGE_REJECT_CAL_PHASE = 0x16.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C unless otherwise noted

**Table 4.**

| Parameter | Rating |
|---|---|
| AVDD, IOVDD, VDDBAT1 and VDDBAT2 to GND | −0.3 V to 3.96 V |
| Digital Input Voltage to GND | −0.3 V to 3.96 V |
| Digital Output Voltage to GND | −0.3 V to 3.96 V |
| $V_{REF}$ to GROUND | −0.3 V to 3.96 V |
| Analog Inputs to GND | −0.3 V to 2.1 V |
| Operating Temperature Range | –40°C to +85°C |
| Storage Temperature Range | –65°C to +150°C |
| Junction Temperature | 105°C |
| $\theta_{JA}$ Thermal Impedance | |
| 64-Pin LFCSP _VQ | 25°C/W |
| ESD (Human Body Model) | ±1.5 kV |
| Peak Solder Reflow Temperature | |
| Pb-Free Assemblies (30 s) | 260°C |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

The exposed paddle of the LFCSP package should be connected to ground.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

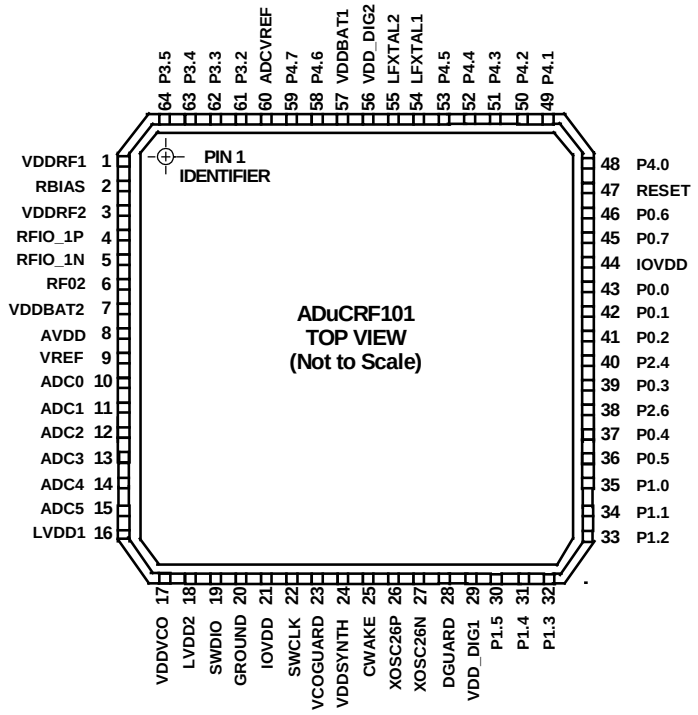



*Figure 8. 64-Lead LFCSP_VQ Pin Configuration*

**Table 5. Pin Function Descriptions**

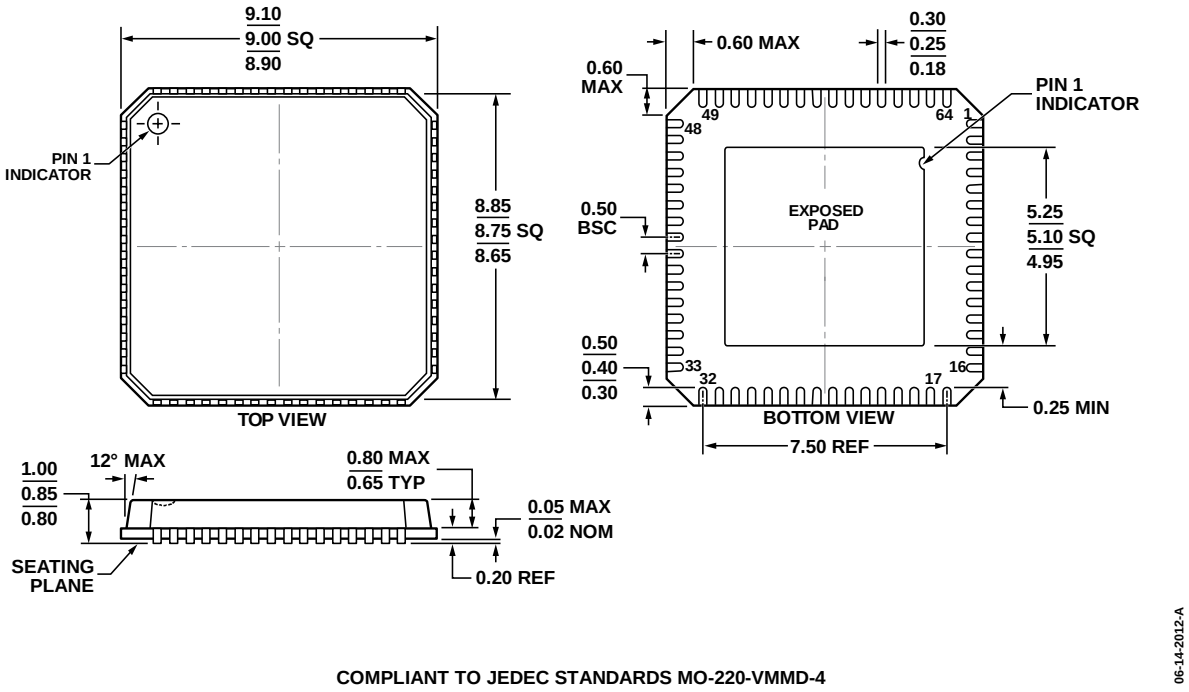
| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | VDDRF1 | Voltage Regulator output for RF block. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection. |
| 2 | RBIAS | External bias resistor. A 36 kΩ resistor with 2% tolerance should be used. |
| 3 | VDDRF2 | Voltage Regulator output for RF block. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection. |
| 4 | RFIO_1P | LNA Positive Input in Receive Mode. Differential PA Positive Output in Transmit Mode. |
| 5 | RFIO_1N | LNA Negative Input in Receive Mode. Differential PA Negative Output in Transmit Mode. |
| 6 | RF02 | Single ended PA output. |
| 7 | VDDBAT2[6] | Battery Terminal, supply for the LDOs used in the RF section of the transceiver. |
| 8 | AVDD[6] | Battery terminal, Supply for analog circuits such as ADC and ADC internal reference, POR, PSM and LDOs. |
| 9 | VREF | Internal 1.25 V ADC reference. A 0.47 µF capacitor between this pin and ground is required. |
| 10 | ADC0 | ADC input channel 0. Input of DIFF0 pair in differential mode. |
| 11 | ADC1 | ADC input channel 1. Input of DIFF0 pair in differential mode. |
| 12 | ADC2 | ADC input channel 2. Input of DIFF1 pair in differential mode. |
| 13 | ADC3 | ADC input channel 3. Input of DIFF1 pair in differential mode. |
| 14 | ADC4 | ADC input channel 4. Input of DIFF2 pair in differential mode. |
| 15 | ADC5 | ADC input channel 5. Input of DIFF2 pair in differential mode. |
| 16 | LVDD1 | On chip LDO decoupling output. Connect a 0.47 µF capacitor to the 1.8V output to ensure core operating voltage is stable. For correct operation a 1 µF capacitor needs to be connected between this pin and LVDD2 (pin 18). |
| 17 | VDDVCO | Voltage Regulator output for VCO. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection. |
| 18 | LVDD2 | On chip LDO decoupling output. Connect a 0.47 µF capacitor to the 1.32V output to ensure core operating voltage is stable. For correct operation a 1 µF capacitor needs to be connected between this pin and LVDD1 (pin 16). |
| 19 | SWDIO | Serial Wire bi-directional data |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 20 | GND | Ground pin, should be connected to the PADDLE. |
| 21 | IOVDD[6] | Battery terminal, General Purpose IO supply. |
| 22 | SWCLK | Serial Wire debug clock |
| 23 | VCOGUARD | Guard, screen for VCO, should be connected to VDDVCO. |
| 24 | VDDSYNTH | Voltage Regulator output for Synthesizer. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection. |
| 25 | CWAKE | External capacitor for wake up control. A 150 nF capacitor should be placed between this pin and ground. |
| 26 | XOSC26P | The 26MHz reference crystal should be connected between this pin and XOSC26N. (HFXTAL) |
| 27 | XOSC26N | The 26MHz reference crystal should be connected between this pin and XOSC26P. (HFXTAL) |
| 28 | DGUARD | Internal Guard, Screen for Digital Cells, should be connected to VDD_DIG1. |
| 29 | VDD_DIG 1 | Voltage Regulator output for Digital. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection. |
| 30 | P1.5/IRQ6/I2CSDA/PWM7 | General Purpose Input and Output Port 1.5/External Interrupt 6/I2C Serial Data/PWM channel 7. |
| 31 | P1.4/IRQ5/I2CSCL/PWM6 | General Purpose Input and Output Port 1.4/External Interrupt 5/I2C Serial Clock/PWM channel 6. |
| 32 | P1.3/PWM5 | General Purpose Input and Output Port 1.3/PWM channel 5. |
| 33 | P1.2/PWM4 | General Purpose Input and Output Port 1.2/PWM channel 4. |
| 34 | P1.1/PORB/ TXD /PWM3 | General Purpose Input and Output Port 1.1/POR output/ UART TXD/ PWM channel 3. |
| 35 | P1.0/RXD/IRQ4/ MOSI /PWM2 | General Purpose Input and Output Port 1.0/UART RXD/ External Interrupt 4/ SPI1 Master Out Slave In Pin (MOSI)/PWM channel 2. |
| 36 | P0.5/$\overline{CS2}$ /ECLKIN | General Purpose Input and Output Port 0.5/SPI1 Chip Select 2/External Clock Input |
| 37 | P0.4/$\overline{CS1}$ /ECLKOUT | General Purpose Input and Output Port 0.4/SPI1 Chip Select 1/External Clock Output. |
| 38 | P2.6 | General Purpose Input and Output Port 2.6. This pin should not be connected. This pin is connected internally to the RF transceiver. It can be used for BER measurements. |
| 39 | P0.3/IRQ1/$\overline{CS0}$ /ADCCONVST/PWM1 | General Purpose Input and Output Port 0.3/External Interrupt 1/SPI1 Chip Select 0/ADC convert start/PWM channel 1. |
| 40 | P2.4/IRQ8 | General Purpose Input and Output Port 2.4. This pin should not be connected. This pin is connected internally to the RF transceiver. It can be used for debug purposes to monitor RF transceiver interrupt/ External Interrupt 8 |
| 41 | P0.2/MOSI/ PWM0 | General Purpose Input and Output Port 0.2/SPI1 Master Out Slave In Pin (MOSI)/PWM channel 0. |
| 42 | P0.1/SCLK | General Purpose Input and Output Port 0.1/SPI1 Serial Clock |
| 43 | P0.0/MISO | General Purpose Input and Output Port 0.0/SPI1 Master In Slave Out Pin (MISO) |
| 44 | IOVDD | General Purpose I/O supply. Connect to the battery terminal |
| 45 | P0.7/IRQ3/$\overline{CS4}$ /CTS | General Purpose Input and Output Port 0.7/ External Interrupt 3 / SPI1 Chip Select 4/ UART hand shake. |
| 46 | BM/P0.6/ IRQ2/$\overline{CS3}$ / RTS/PWM0 | BM (Boot Mode). The ADuCRF101 enters serial download mode if P0.6 is low during an external Reset event. It executes user code after any reset event or if P0.6 is high during an external Reset event. / General Purpose Input and Output Port 0.6/External Interrupt 2/ SPI1 Chip Select 3 / UART hand shake/PWM channel 0. |
| 47 | RESET | Active Low. A low signal on this pin for 24 system clocks will cause the part to reset. |
| 48 | P4.0/PWM0 | General Purpose Input and Output Port 4.0/PWM channel 0. |
| 49 | P4.1/PWM1 | General Purpose Input and Output Port 4.1/PWM channel 1. |
| 50 | P4.2/PWM2 | General Purpose Input and Output Port 4.2/PWM channel 2. |
| 51 | P4.3/PWM3 | General Purpose Input and Output Port 4.3/PWM channel 3. |
| 52 | P4.4/PWM4 | General Purpose Input and Output Port 4.4/PWM channel 4. |
| 53 | P4.5/PWM5 | General Purpose Input and Output Port 4.5/PWM channel 5. |
| 54 | LFXTAL1 | 32.768 kHz watch crystal output for WU timers. |
| 55 | LFXTAL2 | 32.768 kHz watch crystal input for WU timers. |
| 56 | VDD_DIG2 | Voltage Regulator output for Digital section of the transceiver. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection. |
| 57 | VDDBAT1[6] | Battery Terminal, supply for the digital section of the transceiver and GPIOs. |
| 58 | P4.6/PWM6 | General Purpose Input and Output Port 4.6/PWM channel 6. |
| 59 | P4.7/PWM7 | General Purpose Input and Output Port 4.7/PWM channel 7. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 60 | ADCVREF | Transceiver's ADC Reference Output. A 220 nF capacitor should be placed between this pin and ground for adequate noise rejection. |
| 61 | P3.2/PWMSYNC | General Purpose Input and Output Port 3.2/PWM synchronisation. |
| 62 | P3.3/PWMTRIP | General Purpose Input and Output Port 3.3/PWM safety cut off. |
| 63 | P3.4 | General Purpose Input and Output Port 3.4. |
| 64 | P3.5 | General Purpose Input and Output Port 3.5. |
| 65 | PADDLE | The exposed package paddle should be soldered to a metal pad on the PCB, and connected to ground. |

[6] VDDBAT1, VDDBAT2, AVDD and IOVDD should all be connected together.

# OUTLINE DIMENSIONS




**COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4**

*Figure 2. 64-Lead Frame Chip Scale Package [LFCSP_VQ]*
*9 mm x 9 mm Body, Very Thin Quad*
*(CP-64-5)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Description | Package Option |
|---|---|---|---|
| ADUCRF101BCPZ64 | -40°C to 85°C | 12-bit ADC, 164k Byte Flash and 8k Byte SRAM | 64-lead LFCSP |
| ADUCRF101BCPZ128 | -40°C to 85°C | 12-bit ADC, 128k Byte Flash and 16k Byte SRAM | 64-lead LFCSP |
| ADUCRF101CCPZ128 | -40°C to 85°C | 14-bit ADC, 128k Byte Flash and 16k Byte SRAM | 64-lead LFCSP |
| EV-ADuCRF101MK3Z | -40°C to 85°C | Evaluation board for 433 MHz operation | N/A |
| EV-ADuCRF101MK1Z | -40°C to 85°C | Evaluation board for 915 MHz operation | N/A |
| EV- ADuCRF101QSP1Z | -40°C to 85°C | Quick start Plus for 915 MHz operation | N/A |
| EV-ADuCRF101QSP3Z | -40°C to 85°C | Quick start Plus for 433 MHz operation | N/A |

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).


PR09464-0-11/12(PrG).